CLAIMS

What is claimed is:

1. A method of controlling a computer having a plurality of memory buses operating according to a multi-channel mode, comprising:

reading memory information of at least one of a plurality of memory modules connected to the respective memory buses; and

displaying whether the plurality of the memory buses operate in the multi-channel mode by comparing the read memory information with each other.

2. The method of claim 1, wherein the read memory information comprises serial presence detect (SPD) data stored in the respective memory modules.

3. The method of claim 2, wherein the SPD data comprises memory capacity information of the respective memory modules.

4. The method of claim 1, further comprising examining an existence of an arrangement of the memory modules connected to the plurality of the memory buses that allows the plurality of the memory buses to operate in the multi-channel mode, when the comparing determines that the plurality of the memory buses do not operate in the multi-channel mode.

5. The method of claim 4, wherein the displaying whether the plurality of the memory buses operate in the multi-channel mode further comprises displaying the arrangement of the memory modules allowing the plurality of the memory buses to operate in the multi-channel mode.

6. A computer having a plurality of memory buses operating in a multi-channel mode, comprising:

a controller determining whether the plurality of the memory buses operate in the multi-channel mode by comparing memory information of at least one of a plurality of memory modules, connected to the respective memory buses, to each other; and

an output unit providing information whether the plurality of memory buses operate in the multi-channel mode according to the determination by the controller.

7. The computer according to claim 6, wherein the memory information of the memory modules connected to the respective memory buses comprises serial presence detect (SPD) data stored in the respective memory modules.

8. The computer according to claim 7, wherein the SPD data comprises memory capacity information of the respective memory modules.

9. The computer according to 6, wherein the controller examines an existence of an arrangement of the memory modules connected to the plurality of the memory buses that allows the plurality of the memory buses to operate in the multi-channel mode, when the controller determines that the plurality of the memory buses do not operate in the multi-channel mode.

10. The computer according to claim 9, wherein the output unit visually informs the arrangement of the memory modules allowing the plurality of the memory buses to operate in the multi-channel mode.

11. The computer according to claim 10, wherein the controller is a determining program determining whether the plurality of the memory buses operate in the multi-channel mode.

12. The computer according to claim 11, wherein the determining program is stored in a BIOS ROM.

13. The computer according to claim 10, wherein the output unit comprises a monitor to display information about the arrangement.

14. A computer readable storage controlling a computer according to a stored process of:

reading memory information of at least one of a plurality of channeled memory modules connected to respective memory buses;

comparing the read memory information to each other; and

outputting multi-channel mode information of the memory buses based upon the comparing.

15. The computer readable storage of claim 14, wherein the memory information comprises manufacturer information, device structure and logical bank information, type information and capacity information.

16. The computer readable storage of claim 14, wherein the comparing comprises comparing memory capacities of the channeled memory modules to each other to determine if same memory capacity memory modules are separately connected to each memory bus, respectively.

17. The computer of claim 6, further comprising:

a BIOS ROM performing a power on self test (POST) during booting of the computer, and

wherein the controller is software stored in the BIOS ROM and determining the multi-channel mode memory bus operation during the POST.

18. The computer of claim 17, further comprising:

a north bridge controlling the plurality of the memory modules, wherein the controller controls the north bridge to read the memory information during the POST.

19. A method, comprising:

outputting multi-channel mode memory bus information based upon memory information of channeled memory modules.

20. A method of determining a multi-channel mode memory bus operation of a computer having a plurality of memory buses connected to corresponding channeled memory modules, the method comprising:

executing a program to determine the multi-channel mode memory bus operation during a power on self test, the program controlling the computer according to a process of:

reading memory information of at least one of the channeled memory modules connected to the memory buses respectively;

comparing the read memory information to each other; and

displaying whether the memory buses operate in the multi-channel mode according to the comparing of the read memory information; and

displaying an arrangement of the memory modules allowing the multi-channel mode memory bus operation.